



ORIGINAL ARTICLE

ONCLE (One Clock Ensemble) for Galileo's Next-Generation Robust Timing System

Qinghua Wang | Pascal Rochat

Oroliia Switzerland SA (Spectratime)
2000 Neuchâtel, Switzerland

Correspondence

Qinghua Wang, Oroliia Switzerland SA,
Rue du Vauseyon 29, 2000 Neuchâtel,
Switzerland
Email: Qinghua.wang@orolia.com

Abstract

This paper presents the ONCLE (One Clock Ensemble) solution for the Galileo time and frequency reference system with advanced features in terms of robustness, performance, continuity, and simplicity. Each component clock is frequency-steered to the ensemble time, which itself creates an average of those steered clock outputs, while clock faults are detected and corrected in real time within an integrated system. The feasibility of algorithm and hardware approaches has been demonstrated on an elegant breadboard and verified by an extended test and validation campaign at the Engineering Model (EM) level, developed for the Galileo next-generation onboard timing system under European GNSS Evolutions Program. Based on the progress for space application and the heritage on the Galileo ground precise timing facility (PTF), we propose a robust solution for the upgrade of PTF for ground application aiming to provide a fully continuous and performance-improved timescale under automated operation. The capability is demonstrated by preliminary simulation results.

Keywords

algorithm, clock ensemble, GNSS, onboard, robust, time and frequency system

1 | INTRODUCTION

The generation of the clock ensemble output (or timescale), based on a pool of clocks that shows better performance in terms of accuracy, stability and reliability, is a concept that has been successfully implemented over many years. The fundamental concept of the timescale is the weighted average of the N clocks to optimize the ensemble performance with regard to different individual clock performances (Brown, 1991; Stein, 2003; Thomas et al., 1994).

To improve the robustness of the timing system, the identification of clock anomalous behavior has been of great interest. There is a large body of technical literature on detecting discontinuities in time series using various methods based on sliding square windows and Kalman filters (Galleani & Tavella, 2012; Huang et al., 2014; Khare et al., 2016; Riley, 2008; Signorile, 2014; Zenzinger et al., 2012).

To improve performance and robustness, various solutions based on real-time algorithms for clock ensembles (Galleani et al., 2019; Trainotti et al., 2019) and monitoring are possible. In fact, a practical implementation for phase continuous

clock switching has been reported (Bertacco et al., 2020) for ground application. Alternative developments were conducted for the Galileo onboard timing system (Krauss et al., 2014; Soualle et al., 2010).

In this paper, we report our *ONCLE Solution* for the Galileo timing system. By this solution, the unit integrates clock ensembling with automated clock fault handling and switching and generates a timescale or frequency reference physically realized via a steering loop with simple implementation.

Section 2 describes the ONCLE concept. Section 3 provides the development status for the Galileo second-generation onboard timing system with verification testing results obtained at the Engineering Modeling (EM) level. Based on these outcomes, in Section 4, we propose an improved version of the timing system for current precise timing facility (PTF) in the Galileo ground segment, demonstrated by preliminary simulation results. Section 5 gives a conclusion and outlook of the work as a whole.

2 | ONCLE CONCEPT

The concept of the ONCLE (One Clock Ensemble) for a robust time and frequency reference system was initiated by Spectratime in 2009 (Wang & Rochat, 2009). Since then, we have conducted feasibility studies and verifications of algorithm and hardware approaches for both space and ground applications.

With a minimum of three input clocks, the integrated system is able to generate an output signal with improved robustness and performances by advanced features in real time:

- Clock ensemble based on the weighted average
- Clock fault detection and correction based on a cascade of low-pass recursive filters and associated logic
- Steering loop to keep all clocks in phase and on frequency

Aiming for a simple and reliable solution, the algorithms are designed to be implementable by a field-programable gate array (FPGA) for space application or by a simple industrial micro-controller chip for ground application.

3 | ONBOARD TIMING SYSTEM FOR GALILEO SPACE SEGMENT

3.1 | Current Timing System and the CMCU

The onboard timing system, including ultra-stable atomic clocks and the Clock Monitoring and Control Unit (CMCU), is one of the utmost critical payloads of a global navigation satellite system (GNSS). The frequency stability, robustness, and reliability of the timing system output signals have a direct impact on system performance through their contribution to the system ranging error and system availability.

In the first generation of Galileo satellites, one passive hydrogen maser (PHM) and one Rubidium atomic frequency standard (RAFS) operated in a hot redundancy scheme on each spacecraft, and the CMCU selected the clock signal to be distributed (Felbach, 2003). Vulnerabilities and risks of the present onboard timing system have since been identified.

3.2 | Frequency Reference Subsystem (FRS) EBB Predevelopment for the Next Generation

Under the European GNSS Evolutions Program (EGEP), Spectratime with the support of the GMV developed an elegant breadboard (EBB) of the robust onboard Frequency Reference Subsystem (FRS), which was completed in 2014 (Rochat et al., 2012).

The feasibility of the ONCLE concept as an improved CMCU was demonstrated on FRS EBB over the course of this FRS project. The work was reported in the paper by Rochat et al. (2012). The self-standing unit was able to receive and process a number of clock signals and generate an output signal with improved availability and robustness. Tested under various clock degradation scenarios, this unit demonstrated at the breadboard level its capability to autonomously detect, correct, isolate, and remove (or reintroduce) the identified clock with reduced impact on the output signal.

3.3 | CMCU+ EM Development for the Next Generation

During 2015 and 2019, an engineering model (EM) of the next-generation onboard CMCU (referred to as CMCU+) was developed in the frame of the EGEP (Wang & Rochat, 2019). As a subcontract of Airbus Defense and Space, Spectratime contributed 50% of the work for CMCU+. As far as the algorithms' activities are concerned, the algorithm's design, development, and high-level verification were the responsibility of Spectratime and the implementation of the algorithms on the hardware platform was the responsibility of Airbus (while keeping full functional compatibility with current CMCU).

The algorithm subsystem represents the "+" of the CMCU+ design with advanced features. The algorithms consist of three functionalities processing in real time. The algorithm architecture is based on FRS development and was adapted with CMCU hardware architecture.

FIGURE 1 shows the functional blocks of algorithms and the interface with other blocks and telecommands with signal flow.

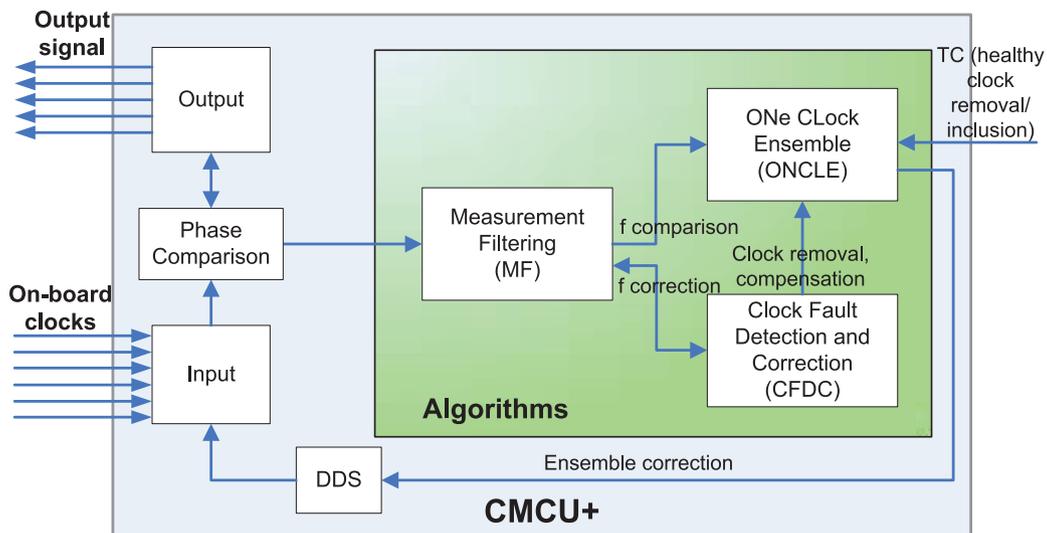


FIGURE 1 Algorithms' functional blocks within basic CMCU+ architecture

Phase comparisons between the output signal of CMCU+ and input signals from onboard clocks go through the Measurement Filtering (MF) algorithm to the ONCLE and Clock Fault Detection and Correction (CFDC) algorithms. In the case of clock faults, the CFDC algorithm provides fault corrections, failed clock removal, and discontinuity compensation commands to MF and the ONCLE. The ONCLE receives telecommands, if necessary, to remove or include a healthy clock and further provides ensemble corrections on the Direct Digital Synthesizer (DDS) to input modules. All input clocks are kept in phase and frequency to the corrected master clock.

The algorithm design was first verified by the authors using a simulation under various test cases with three clock scenarios including events on master and secondary clocks. After the implementation of the algorithms, high-level performance verification was conducted at the CMCU+ EM level in real-time operation with two sets of input Atomic Frequency Standard (AFS) configurations to assure the atomic clock technology diversity:

- AFS Set A: 1 x PHM + 3 x RAFS
- AFS Set B: 3 x PHM + 1 x RAFS

According to the high-level performance verification requirements for CMCU+, various test cases of ensemble stationary performance and transient performances of clock events (healthy clock removal or inclusion, different dynamic frequency jumps, white frequency noise [WFN] level increase, clock failures, etc.) have been performed. Test results were verified by the clock-handling capability, Allan Deviation (ADEV), and the Maximum Accumulated Phase Offset (MAPO) during 100 mins of the output signal, in which the 100 min was driven by the time between two consecutive updates of the broadcast navigation message in the Galileo system (refer to ESA [n.d.]).

The FemtoSteppers were used to create frequency and phase steps as testing and validation tools to replay real clock measurement data or typical clock model files and to generate typical clock anomalies, with a resolution of 100 fs in phase and $1e-17$ in frequency. Figure 2 illustrates the block diagram of the test bench. FemtoSteppers were connected to four active inputs of the CMCU+ unit to replace four atomic clocks. Two Timepods were used to measure the frequency or phase performance of signals: One for CMCU+ output and the other for that of input clock signals, in particular, where clock events occur. The CMCU+ EM under testing with the test bench is shown in Figure 3.

A few test cases are presented below as examples (refer to the paper by Wang and Rochat [2019]) for more test results). Figure 4 shows test cases of the ensemble stationary performance with two AFS scenarios:

- For Set A, the ADEV of the CMCU+ output was dominated by the master clock (PHM01). The high performance of the PHM was maintained in the ensemble output while the sub-ensemble of 3x RAFS assured the full detection capability and the capability to form a next ensemble in case of the master PHM anomaly or failure.
- For Set B, the ADEV at 1 s of the CMCU+ output was dominated by that of the individual PHM which served as the master clock and was improved when comparing individual PHMs at $\tau \geq 10$ s. The theoretical improvement limit was $1/\sqrt{N}$ (N being the number of clocks) when the ensemble driving clocks were of the same quality.

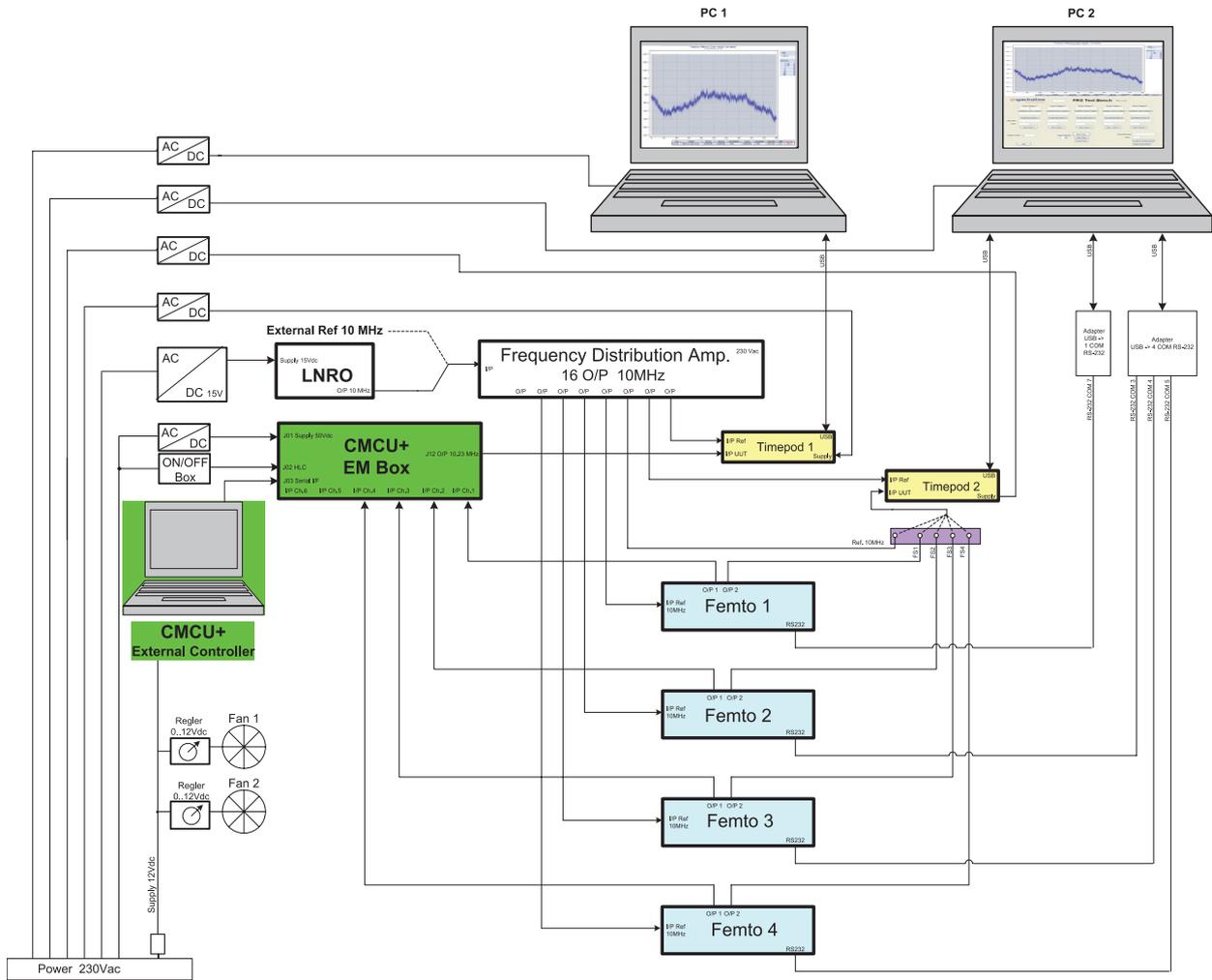


FIGURE 2 Block diagram of the test bench for the CMCU+ EM high-level performance verification tests



FIGURE 3 CMCU+ EM (right) under testing with the test bench (left); (top-right: EM external controller PC; middle-right: EM box; bottom-right: Power supply and high-level command ON/OFF box)

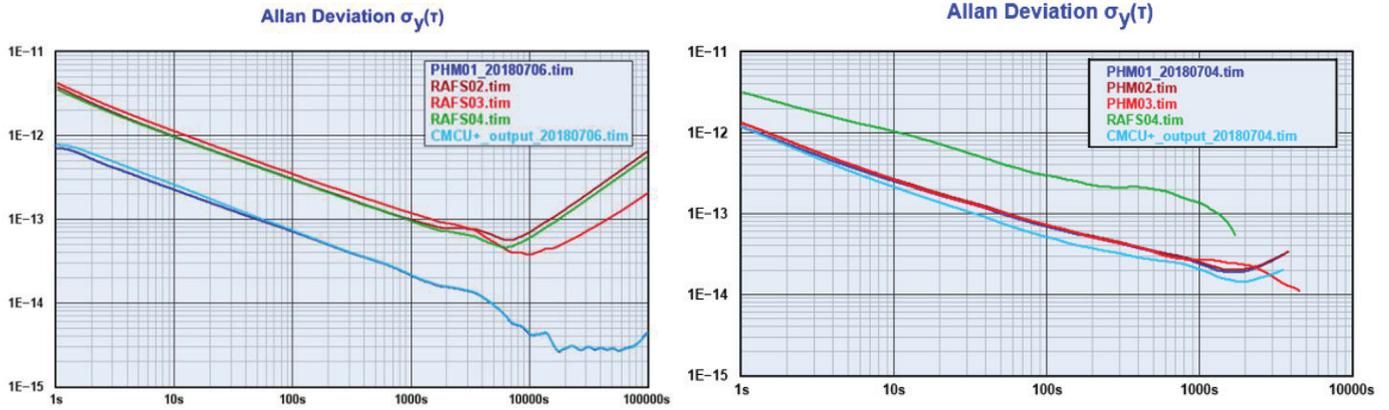


FIGURE 4 ADEV of CMCU+ output (for AFS Set A on the left and AFS Set B on the right)

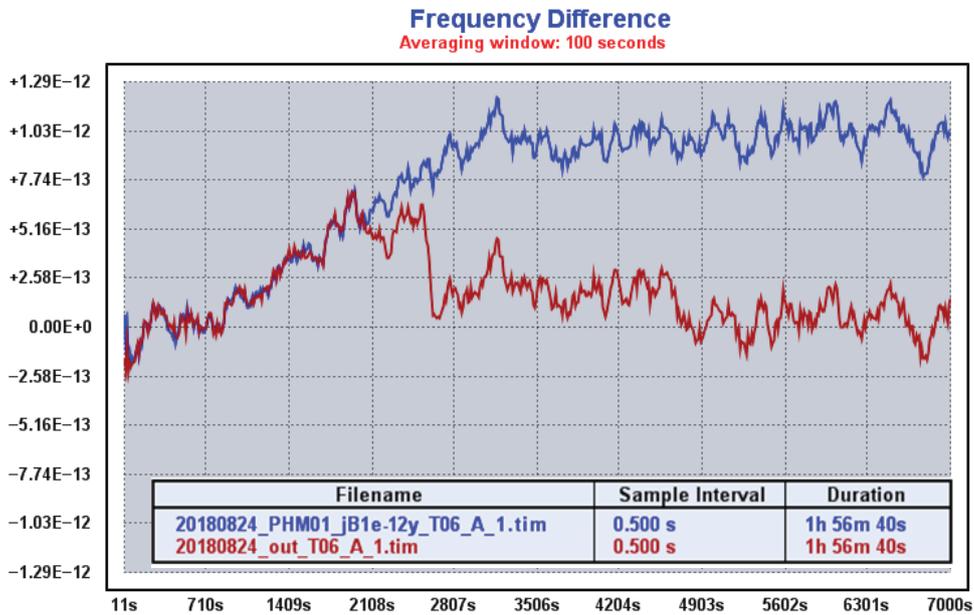


FIGURE 5 Test case: Medium-dynamic frequency jump on master PHM01 for AFS Set A

Figure 5 shows the test case when a medium-dynamic frequency jump of $1e-12$ during 2,500 s started at 500 s on the master PHM01 for AFS Set A corresponding to the MAPO on PHM01 of 4.8 ns during 100 min. The CMCU+ output frequency was corrected consequently at 2,048 s, 2,540 s, and 4,689 s, triggered by small and medium jump detectors. The MAPO of the CMCU+ output during the 100 min was reduced to 1.1 ns (within the limit of 1.2 ns) during the anomaly specified for CMCU+. It demonstrated that the detection and correction of the jump is useful as long as it is performed adequately before the next update of the navigation message within 100 min.

Figure 6 shows the test case when the white frequency noise (WFN) level increased by 10 times starting at 500 s on the master PHM01 for AFS Set A. The anomaly on PHM01 was shortly detected in 53 s by the large jump detector. The master PHM01 was immediately removed and switched over. The output frequency was affected only during these 53 s and was representative of the ensemble of 3x RAFS. The MAPO of CMCU+ output over the 100-min duration remained below 0.28 ns.

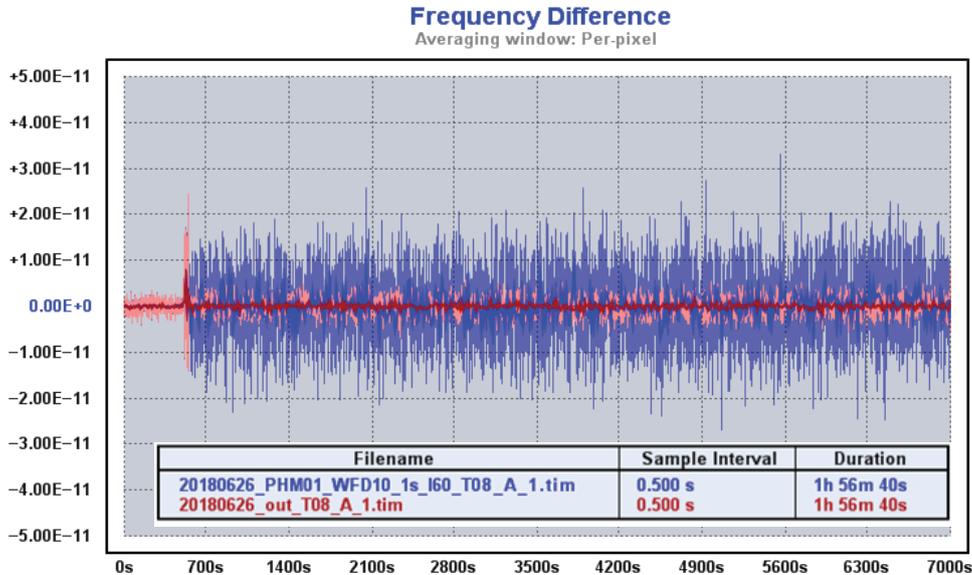


FIGURE 6 Test case: WFN level increase on master PHM01 for AFS Set A

4 | TIMING SYSTEM FOR GALILEO GROUND SEGMENT

4.1 | Current PTF

The precise timing facility (PTF) is a key element of the ground mission segment to generate Galileo System Time (GST). The active hydrogen maser (AHM) provides the physical realization of GST, ensuring the extremely high short-term stability required for navigation purposes (Morante et al., 2016; Stehlin et al., 2006; Zanello et al., 2009).

In order to reinforce GST availability, the PTF is designed to operate with at least two AHMs (one as primary and the other as backup). The backup AHM steering algorithm was developed to steer the backup AHM in phase to the primary AHM (Wang et al., 2008). In case of signal loss or out-of-lock of the primary AHM, the automatic clock switching was implemented to ensure GST (master clock [MC]) continuity by switching to the backup AHM (Zanello et al., 2009).

Several algorithms have been implemented in PTF to identify performance anomalies in GST(MC) and clocks as phase and frequency jumps and instabilities. When a clock anomaly occurs, the output of the algorithm exceeds the threshold and a warning is raised, offered by the measurement function (Zanello et al., 2009).

However, in this configuration, the detection of above clock anomalies as phase and frequency jumps and instabilities (including other lower-dynamics clock failure mechanisms than clock signal loss or out-of-lock) was not followed by automatic fault correction or clock switch-over, so human intervention was required, which could have been detrimental to the continuity of the GST. The other limitation of the current PTF was that the short-term stability of the GST relies on the individual nominal AHM.

4.2 | Proposal of Robust Clock Ensemble for Next Generation

The results and experiences gathered for an onboard timing system led us to propose a Robust Clock Ensemble (RCE) solution for the next generation of PTF,

which aims to integrate time generation as well as measurement and control subsystems (Wang et al., 2015). The ONCLE-based solution aims to improve the performance of GST, real-time clock anomaly detection, and automatic fault compensation (or clock switch-over). In particular, it will avoid the discontinuity in frequency and phase of the output signal to GST to enable reliable satellite clock modeling, which is essential to support the navigation timekeeping performance which is the key purpose of the PTF.

A mathematical model was developed to simulate the expected RCE output versus four AHM inputs. The function of phase-locked loop (PLL) based on the FemtoStepper, the phase comparator, and the proportional integral (PI) filter, as well as the functions of ONCLE and CFDC, were established in the model. Figure 7 shows the architecture of RCE covering the proposed hardware and algorithms. The RCE output is defined by the master clock, steering by the algorithms, and correction via the output Femtostepper.

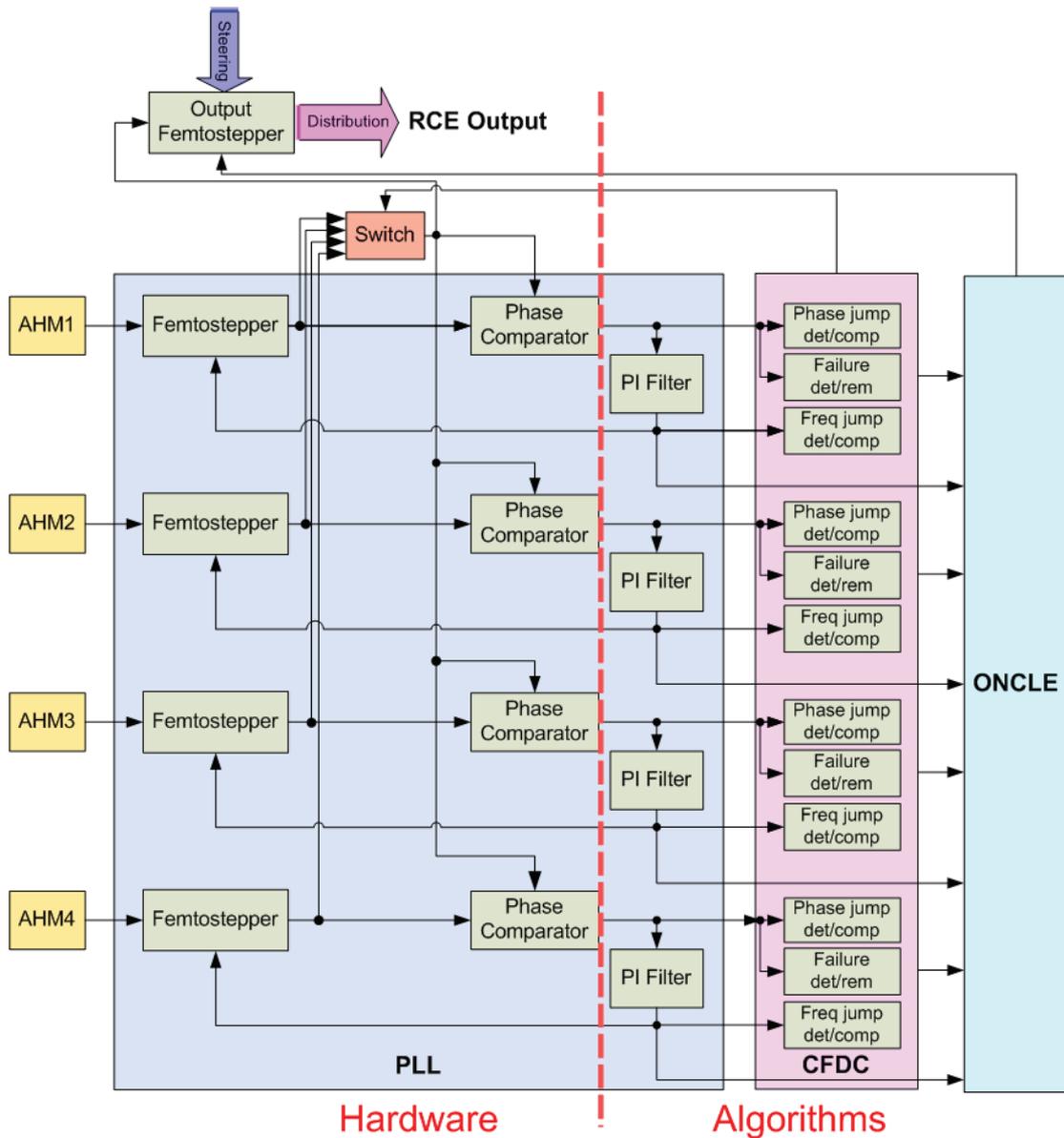


FIGURE 7 Architecture of the proposed RCE for physical realization of GST for next-generation PTF

4.2.1 | PLL

Figure 8 shows the architecture of the steering system, forming a basic PLL. The PI filter acquires the phase difference between the secondary and master clocks and generates a steering frequency correction to be applied to the secondary clock via the FemtoStepper. The s-transfer function of second-order closed loop is:

$$C(s) = \frac{2\xi\tau s + 1}{\tau^2 s^2 + 2\xi\tau s + 1} \quad (1)$$

where τ is the loop time constant of 1,000 s, selected as a trade-off of the time offset and the frequency stability to allow smooth steering of secondary clocks; ξ is the damping factor, which was set to 1.

Figure 9 demonstrates that the secondary clock AHM2 is steered in-phase with the master clock AHM1 from the simulation.

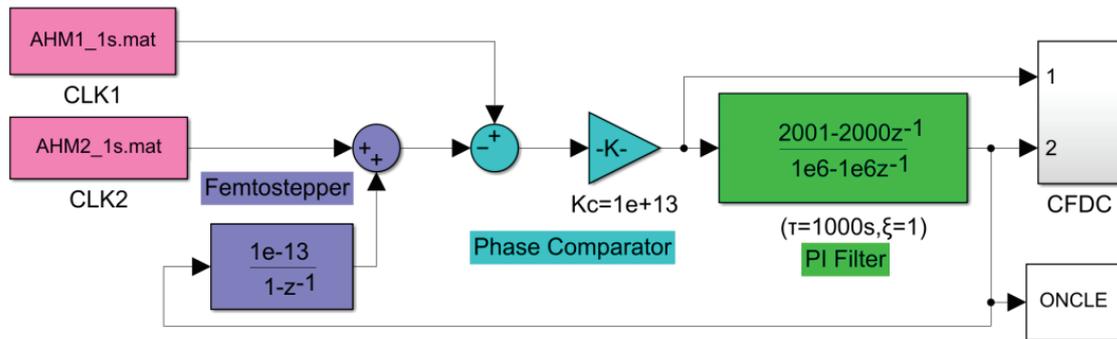


FIGURE 8 Simulation model of the PLL with PI filter algorithm

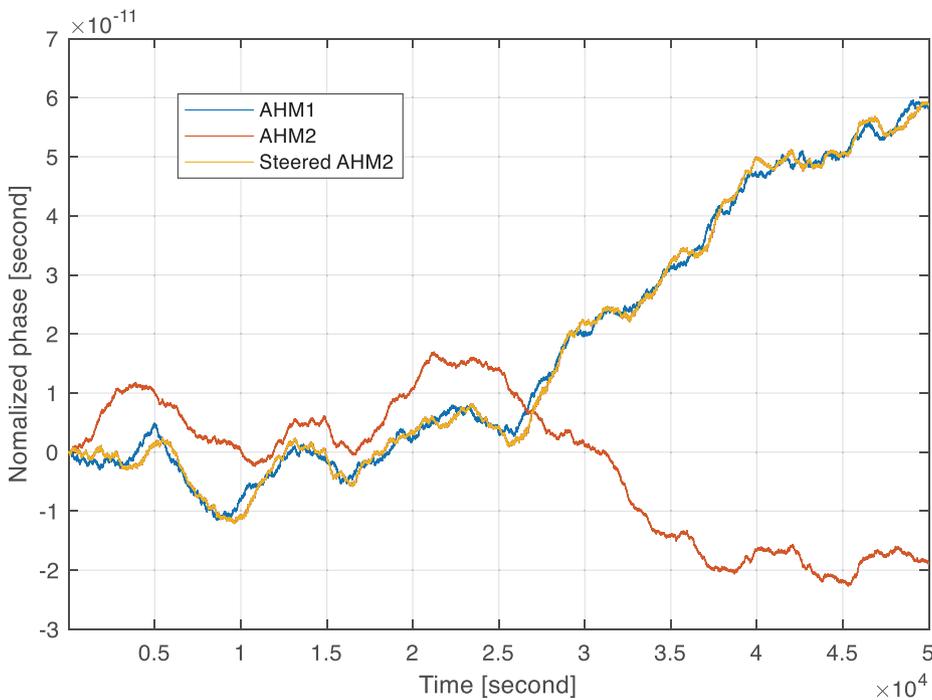


FIGURE 9 Phases of the master AHM1, the free-running AHM2, and the steered AHM2

4.2.2 | ONCLE

The ensemble generation algorithm is based on the weighted or simple average of clocks, shown in Figure 10. Adaptive weights may be envisaged to be applied on input clocks. The frequency of the master clock is corrected to generate an ensemble output signal. Then, each clock is phase and frequency corrected and aligned to each input channel to the weighted average of individual clocks.

The ADEV comparison over 10 days' data in Figure 11 demonstrated improvement with the ensemble. The RCE output achieved the flicker floor of ADEV at 6×10^{-16} . The frequency drift of RCE was $6.4 \times 10^{-16}/\text{day}$, the average of the four AHMs. The output drift was also adjustable via the FemtoStepper by the correction command.

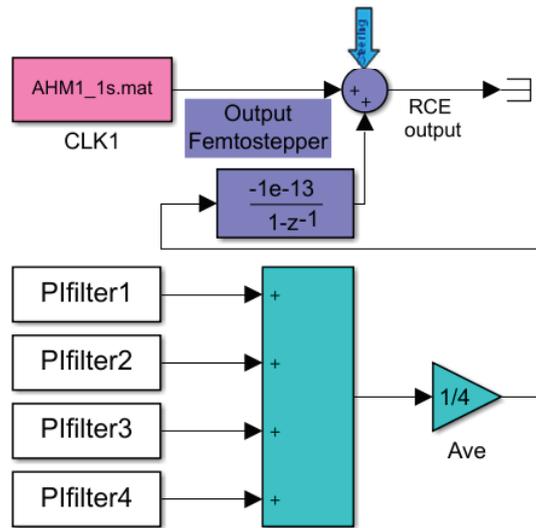


FIGURE 10 Simulation model of the ONCLE algorithm with RCE output

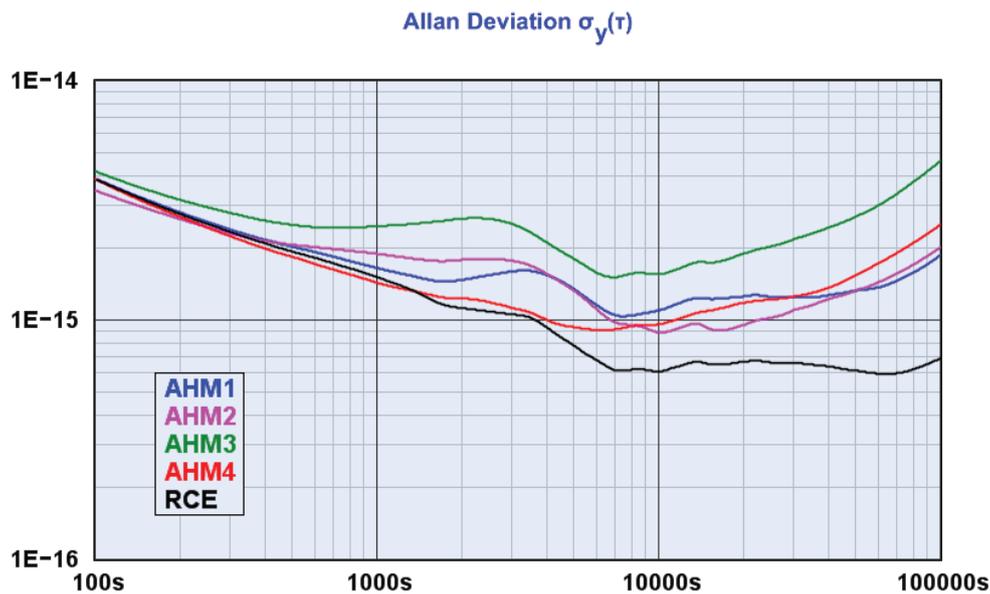


FIGURE 11 Frequency stability in ADEV (including drift) for four individual AHM's and RCE output (simulation results)

4.2.3 | CFDC

The CFDC aims for the reliable detection and correction of clock faults with simple approaches. Figure 12 illustrates three functions handling main clock fault types:

- Phase jump detection and compensation
- Clock failure fast detection and clock removal
- Frequency jump detection and compensation

The phase measurements per 1 s from the phase comparator gives a straightforward indication in the case of a phase jump. Once a phase jump exceeds the pre-defined threshold, the compensation function makes the phase correction on the level of one threshold to the input with a 1-s delay and iterates the comparison for the next correction. As shown in Figure 13, the phase jump of 30 ps was detected immediately in 1 s after the event occurrence and was fully corrected during the next few seconds.

The frequency jump detection is based on recursive filters with different filtering factors, which requires minimal memory and registers, and is efficient for the detection of frequency jumps in various dynamics.

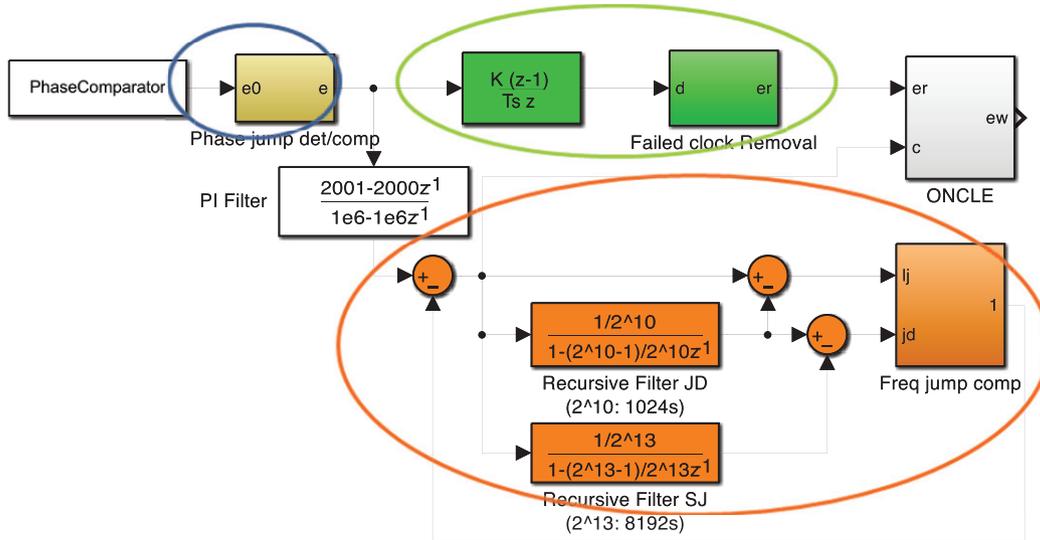


FIGURE 12 Simulation model of the CFDC algorithms

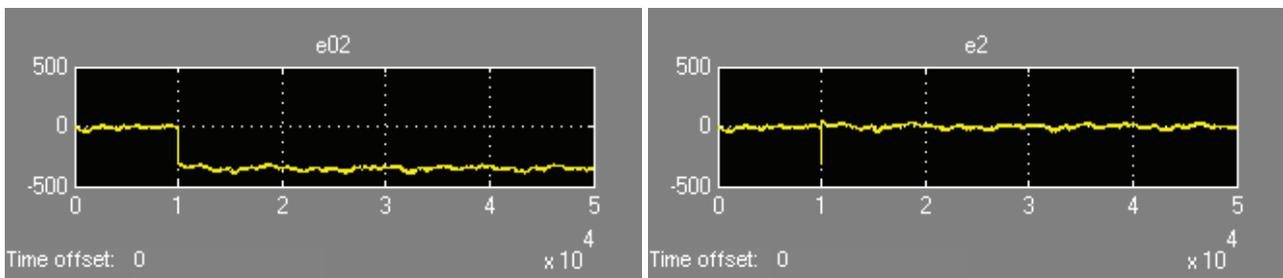


FIGURE 13 Correction of phase jump of 30 ps; y-axis represents phase difference [step] after phase comparator and the x-axis represents time in seconds (left: without correction; right: with correction)

The difference equation of the first-order low-pass recursive filter (e.g., the Infinite Impulse Response [IIR] Filter) is:

$$y(n) = \frac{1}{N}x(n) + \frac{N-1}{N}y(n-1) \quad (2)$$

where n is the number of samples, $x(n)$ is the input of the filter, $y(n)$ is the output of the filter, and N is the filtering factor.

The time constant of an exponential moving average is the amount of time for the smoothed response of a unit set function to reach $1 - 1/e \approx 63.2\%$ of the original signal. The relationship between this time constant Tau and the filtering factor N is given by the formula:

$$1/N = 1 - e^{-T_s/Tau} \quad (3)$$

where T_s is the sampling time interval of the discrete time implementation. If the sampling time is fast compared to the time constant, then:

$$Tau \approx N \cdot T_s \quad (4)$$

In each clock input channel, the low-pass recursive filters provide averaged frequencies in different time constants in order to detect various levels of anomalies. The subtraction of two successive filters acts as a high-pass filter and outputs to the fault detection and correction compared to the predefined threshold of each detector. A high-frequency jump can be detected quicker, while the detection of a small jump takes longer. The detection capability is the trade-off of the time constant, the detection time before corrective action, and the detectable level corresponding to noise level of clock technology in the ensemble.

The simulation result of the clock failure with a frequency jump of $8e-12$ is illustrated in Figure 14. The RCE output was not affected by the clock failure as a consequence of the fast detection, discontinuity compensation, and clock removal. The algorithm is capable of detecting a failure of the master or secondary clocks and can switch the master clock to the next healthy clock smoothly.

Figure 15 demonstrates that a very small frequency jump of $1e-14$ is detectable and corrected.

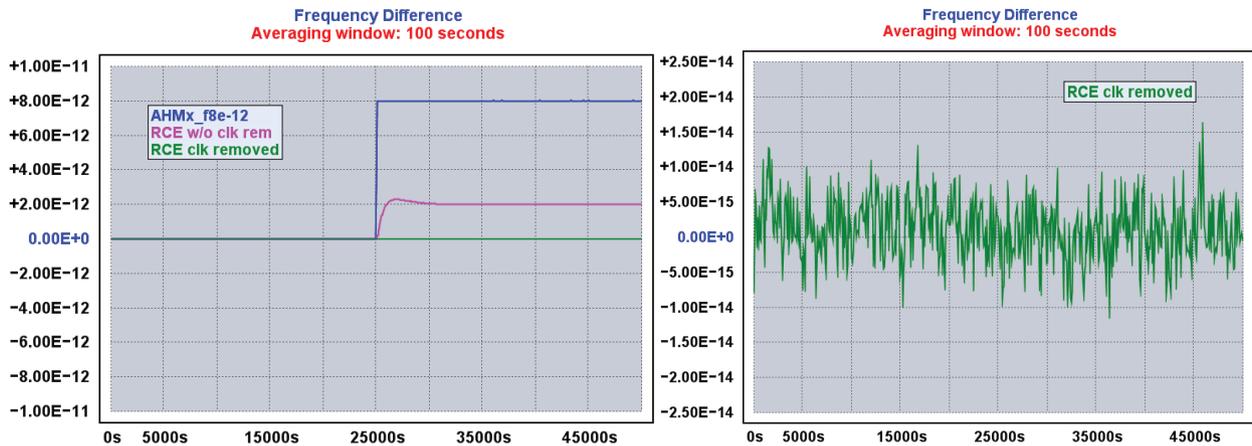


FIGURE 14 Removal of failed clock with frequency jump of $8e-12$ occurred at 25,000 s (left: frequencies of the failed clock and RCE without/with clock removal; right: zoom-in of frequency of RCE with clock removal)

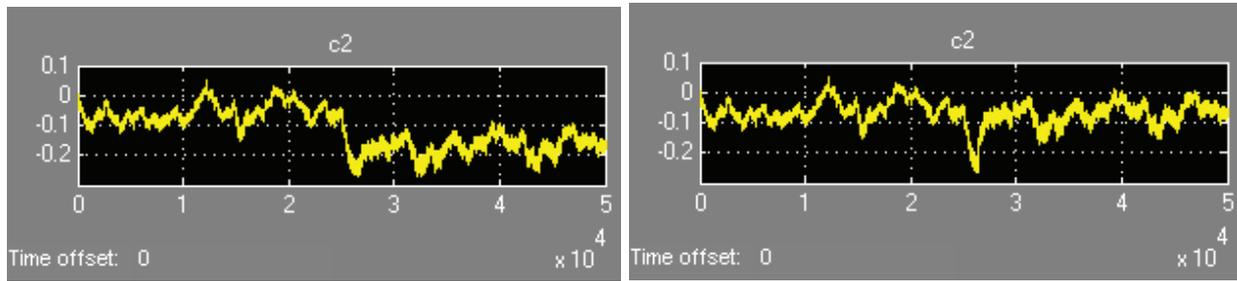


FIGURE 15 Correction of frequency jump of $1e-14$ where the y-axis is the frequency difference output [step] after PI filter and the x-axis is time in seconds (left: without correction; right: with correction)

It is worthwhile to note that frequency jump detection is based on several recursive filters. More filters can be added, if necessary, and optimized depending on system requirements and clock characteristics. The performance of the CFDC in terms of detection delay, false alarm probability, and the minimum detectable level shall be further analyzed for this application in future work.

5 | CONCLUSION

Thanks to the EGEP for next-generation onboard timing system developments, the feasibility of algorithm and hardware approaches to realize the ONCLE concept was demonstrated on the FRS EBB. The output signal with improved robustness and performance was verified by an extended test and validation campaign at the CMCU+ EM level.

Benefits of a robust onboard timing system for the second generation of Galileo (G2G) satellites have been demonstrated, in particular, with the ability to detect and correct space clock anomalies, keeping the latest uploaded navigation clock model valid in case of clock failure, clock removal, or clock inclusion. The clock model stays valid in the case of clock introduction if the clock exhibits standard drift rate with any offset. The only constraint when the new clock is introduced is the wait for clock stabilization after warm-up.

Advantages of the ONCLE solution render it a prospective candidate for an upgrade of the PTF on ground to obtain a continuous GST with improved performance. Preliminary simulation results with four high-performance AHMs have demonstrated the capabilities to provide a robust timescale generation. Moreover, without the need of human intervention, this integrated solution is expected to simplify the operation and, thereby, reduce the operational cost for ground segments.

It is worthwhile to note that this approach may also be interesting for other robust timescale generations on ground in the context of timing metrology. A single device integrating hardware and algorithms for key timescale generation functions (clock comparison, clock ensemble, clock switching, clock anomaly detection, isolation, and recovery) as developed for the onboard CMCU+ but requiring higher performance, should be targeted for the future development.

ACKNOWLEDGMENTS

The authors acknowledge the European Space Agency for the technical guidance on algorithm development for the onboard timing subsystem for Galileo. The authors would like to thank GMV and Airbus DS for collaborations in FRS EBB and CMCU+ EM developments.

Works of FRS and CMCU+ reported in this paper have been supported under contracts of the European Space Agency in the frame of the EGEP. The views presented in the paper represent solely the opinion of the authors and should be considered as R&D results not necessarily impacting the present European Geostationary Navigation Overlay Service (EGNOS) and Galileo system design.

REFERENCES

- Bertacco, E. K., Calonico, D., Cantoni, E., Cerretto, G., Costa, R., Fiasca, F., Formichella, V., Levi, F., Mura, A., Perucca, A., Pizzocaro, M., Pollastri, F., Sellone, M., Sesia, I., Signorile, G., Terzi, P., Thai, T. T., Costanzo, G. A., & Rovera, G. D. (2020). Latest improvements at INRIM time laboratory. *Proc. of the 51st Annual Precise Time and Time Interval Systems and Applications Meeting*, San Diego, CA, 159–168. <https://doi.org/10.33012/2020.17296>
- Brown, K. R. (1991). The theory of the GPS composite clock. *Proc. of the 4th International Technical Meeting of the Satellite Division of the Institute of Navigation (ION GPS 1991)*, Albuquerque, NM, 223–242. <https://www.ion.org/publications/abstract.cfm?articleID=4867>
- European Space Agency (ESA). (n.d.) *Galileo system*. https://www.esa.int/Applications/Navigation/Galileo/Galileo_system
- Felbach, D., Heimbueger, D., Herre, P., & Rastetter, P. (2003). Galileo payload 10.23 MHz master clock generation with a Clock Monitoring and Control Unit (CMCU). *IEEE International Frequency Control Symposium and PDA Exhibition Jointly with 17th European Frequency and Time Forum*, Tampa, FL, 583–586. <https://doi.org/10.1109/FREQ.2003.1275156>
- Galleani, L., & Tavella, P. (2012). Detection of atomic clock frequency jumps with Kalman filter. *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, 59(3), 504–509. <https://doi.org/10.1109/TUFFC.2012.2221>
- Galleani, L., Signorile, G., Formichella, V., & Sesia, I. (2019). Generating a real-time time scale with an ensemble clock and a primary frequency standard. *2019 Joint Conference of IEEE International Frequency Control Symposium and European Frequency and Time Forum*, Orlando, FL. <https://doi.org/10.1109/FCS.2019.8856076>
- Huang, X., Gong, H., & Ou, G., Detection of weak frequency jumps for GNSS onboard clocks. *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*. 61(5), 747–755. <https://doi.org/10.1109/TUFFC.2014.2967>
- Khare, A., Arora, R., Banik, A., & Mehta, S. D. (2016). Autonomous Rubidium clock weak frequency jump detector for onboard navigation satellite system. *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, 63(2), 326–335. <https://doi.org/10.1109/TUFFC.2015.2508939>
- Krauss, P. A., Zenzinger, A., & Fischer, S. (2014). Robust timing subsystem—Generating the next generation timing signal. *Proc. of the 27th International Technical Meeting of the Satellite Division of the Institute of Navigation (ION GNSS+ 2014)*, Tampa, FL, 3380–3388. <https://www.ion.org/publications/abstract.cfm?articleID=12460>
- Morante, Q., Cretoni, D., Putorti, G., Varriale, E., Bianchi, M., Cantelmo, C., Baig, J. F., Nogues, J. F., Aouad, A. T., Siccardi, M., Mudrack, A., & Schlarmann, B. (2016). Performance results of the Galileo precise timing facility. *2016 IEEE Metrology for Aerospace (MetroAeroSpace)*, Florence, Italy, 484–488. <https://doi.org/10.1109/MetroAeroSpace.2016.7573263>
- Riley, W. J. (2008). Algorithms for frequency jump detection. *Metrologia*, 45, S154–S161. <http://dx.doi.org/10.1088/0026-1394/45/6/S21>
- Rochat, P., Droz, F., Wang, Q., & Froidevaux, S. (2012). Atomic clocks and timing systems in global navigation satellite systems. *The European Navigation Conference*, Gdansk, Poland. https://www.rolia.com/wp-content/uploads/2021/07/GNSS_Atomic_Clocks-1.pdf
- Signorile, G. (2014). Analysis of a Kalman filter detector for atomic clock anomalies. *2014 XXXIth URSI General Assembly and Scientific Symposium (URSI GASS)*, Beijing, China. <https://doi.org/10.1109/URSIGASS.2014.6928990>
- Soualle, F., Beck, T., Trautenberg, H., Felbach, D., Stopficken, L., Wendel, J., Fernandez, F. A., Fernandez, A., & Sanchez Nogales, M. (2010). New concept for the on-board master clock generation unit for future Galileo satellites. *Proc. of the 2010 International Technical Meeting of the Institute of Navigation*, San Diego, CA, 880–894. <https://www.ion.org/publications/abstract.cfm?articleID=8869>
- Stehlin, X., Wang, Q., Jeanneret, F., Rochat, P., & Detoma, E. (2006). Galileo system time physical generation. *Proc. of the 38th Annual Precise Time and Time Interval Systems and Applications Meeting*, Reston, VA, 395–406. <https://www.ion.org/publications/abstract.cfm?articleID=13664>
- Stein, S. R. (2003). Time scales demystified. *IEEE International Frequency Control Symposium and PDA Exhibition Jointly with the 17th European Frequency and Time Forum*. Tampa, FL, 223–227. <https://doi.org/10.1109/FREQ.2003.1275093>
- Thomas, C., Wolf, P., & Tavella, P. (1994). Time scales, BIPM. *Monographie*, 94(1). <https://www.bipm.org/en/publications/other-monographies>

- Trainotti, C., Schmidt, T. D., & Furthner, J. (2019). Simulating the realization of a mixed clock ensemble. *2019 Joint Conference of IEEE International Frequency Control Symposium and European Frequency and Time Forum*, Orlando, FL. <https://doi.org/10.1109/FCS.2019.8856103>
- Wang, Q., Rochat, P., & Stehlin, X. (2008). Backup hydrogen maser steering system for Galileo precise timing facility. *International Journal of Navigation and Observation*, 730284. <https://doi.org/10.1155/2008/730284>
- Wang, Q., & Rochat, P. (2009). An anomaly clock detection algorithm for a robust clock ensemble. *Proc. of the 41st Annual Precise Time and Time Interval Systems and Applications Meeting*, Santa Ana Pueblon NM, 121–129. <https://www.ion.org/publications/abstract.cfm?articleID=10678>
- Wang, Q., Droz, F., & Rochat, P. (2015). Robust clock ensemble for time and frequency reference system. *2015 Joint Conference of the IEEE International Frequency Control Symposium & European Frequency and Time Forum*, Denver, CO, 374–378. <http://doi.org/10.1109/FCS.2015.7138861>
- Wang, Q., & Rochat, P. (2019). Algorithms development and verification for next generation on-board clock monitoring and control unit. *2019 Joint Conference of IEEE International Frequency Control Symposium & European Frequency and Time Forum*, Orlando, FL. <https://doi.org/10.1109/FCS.2019.8856006>
- Zanello, R., Blanch, M., Piras, C., Detoma, E., Capetti, P., Bellotti, A., & Villabruna, D. (2009). Implementing the Galileo Precise Timing Facility. *2009 IEEE International Frequency Control Symposium Joint With the 22nd European Frequency and Time Forum*, Besancon, France. <http://doi.org/10.1109/FREQ.2009.5168263>
- Zenzinger, A., Bartusch, T., Kuehl, C., Fischer, S., & Shrestha, A. (2012). Failure detection and correction for clock ensemble in space. *2012 6th ESA Workshop on Satellite Navigation Technologies (Navitec 2012) & European Workshop on GNSS Signals and Signal Processing*, Noordwijk, Netherlands. <https://doi.org/10.1109/NAVITEC.2012.6423054>

How to cite this article: Wang, Q., & Rochat, P. (2022). ONCLE (One Clock Ensemble) for Galileo's next-generation robust timing system. *NAVIGATION*, 69(3). <https://doi.org/10.33012/navi.536>